The Intel® Pentium® M processor
Power-Awareness Story
From Theory to Practice

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Technion EE,
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Based on...

The Intel® Pentium® M Processor: Microarchitecture and Performance

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Located on Israel's Mediterranean coast, Haifa is the home of Intel's Israel Development Center (IDC).

IDC was established in 1974, and is Intel's first development center outside the US. The center is a multi-disciplinary team, with more than 1000 employees.

Many of Intel's leading products were developed and originated at IDC.

IDC's employees are currently working on Intel's future microprocessors, CAD tools, advanced networking components and software technologies.
Announcing Intel® Centrino™ mobile technology. Intel has expanded its history of innovation with new notebook capabilities designed specifically for the mobile world. Now you can work, play and connect without wires. And choose from a whole new generation of thin, light notebooks designed to enable extended battery life.

This new innovative technology enables:
- Integrated wireless LAN capability
- Breakthrough mobile performance
- Extended battery life
- Thinner, lighter designs
Agenda

- The Theory
  - Power, Energy
  - Power Awareness

- The Practice
  - The Intel Pentium M processor micro-architecture

- The Performance
Power and the digital world...

- Power is consumed:
  - When capacitance is charged and discharged.
  - A charged cap is a logical ‘1’, a discharged cap is ‘0’.

- The capacitance can be the gates of other transistors or wires (busses and long interconnects).
Power and the digital world (2)...

- Secondary effects like leakage and short-circuit current are increasing with advanced process technologies.

- Leakage is growing dramatically—Reaching 20% in current process technology, and growing...

- Depends heavily on operating voltage and temperature

Leakage (sub-threshold)

Short-circuit
Power & Energy

• **Total energy**
  - Total of all switch energy and leakage waste
  - Measured in either in joules or watt x hour

• **“Energy per task”**
  Lower Energy per task means
  - Longer battery life.
  - Lower electric bills

• **Power = energy / time = \( \alpha CV^2f \) (+ leakage power)**
  (\( \alpha \): activity, \( C \): capacitance, \( V \): voltage, \( f \): frequency)
  - Measured in watts
Power & Energy

- **Average power**
  - Total energy / Total time
  - Including low-activity and idle-time

- **Peak power**
  - Higher power $\Rightarrow$ higher current.
  - Higher power $\Rightarrow$ higher temperature.
    - Cannot exceed the thermal constrains.

- **Typical figures (leading edge processors)**
  - Average power: 1W-3W
  - Peak power: 20W-100W
Power Density

- Think of watts/cm².
- Denser power is harder to cool.
- Complex algorithms lead to denser power:
  - Dense random logic.
  - Timing pressure leads to faster/bigger/power-hungrier gates.
- Increased every process technology generation (higher power @ smaller die size).
Power Density and Thermal

Power Density (Simulated)\(^1\)
Color codes: (lowest) black, red, orange yellow, white (highest)

Thermal Map (EDO System)\(^2,3\)
(lowest) blue, green, yellow, orange, purple, white (highest)

Pentium M Processor power density example

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\(^1\) Source: Intel® Pentium® M Processor Power Estimation, Budgeting, Optimization, and Validation
Dani Genossar, Nachum Shamir, ITJ Q2/2003

\(^2\) Source: Dani Genossar, Nachum Shamir, Intel 2003

\(^3\) The L2 left portion thermal map blank due to measurements limitations.
Voltage, Power, Frequency

- Transistor switches faster at higher voltage
  - higher voltage enables higher frequency
- Maximum frequency grows about linearly with voltage.
  ...Within a given voltage range Vmin-Vmax.
  - $V < V_{\text{min}}$
    - transistors won’t switch.
  - $V > V_{\text{max}}$
    - the device may burn.
- “The cube law”:
  $P \approx kV^3$
  (or $\sim 1\%V = 3\%P$)
- Implications
  - Can save energy/power when Performance is not a factor

* Source: Intel Corp. (http://developer.intel.com)
## Bean Counting*

<table>
<thead>
<tr>
<th></th>
<th>High Voltage</th>
<th>Low Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. Number of transistors</strong></td>
<td>80 M</td>
<td>80 M</td>
</tr>
<tr>
<td><strong>2. Die area</strong></td>
<td>80 mm²</td>
<td>80 mm²</td>
</tr>
<tr>
<td><strong>3. Operation Voltage</strong></td>
<td>1.48 V</td>
<td>0.96 V</td>
</tr>
<tr>
<td><strong>4. Operation frequency</strong></td>
<td>1.6 GHz</td>
<td>0.6 GHz</td>
</tr>
<tr>
<td><strong>5. Energy per switch per transistor</strong></td>
<td>0.85 fJ</td>
<td>0.36 fJ</td>
</tr>
<tr>
<td><strong>6. Power per transistor (#4x#5)</strong></td>
<td>1.4 uW</td>
<td>0.21 uW</td>
</tr>
<tr>
<td><strong>7. Activity factor</strong></td>
<td>20%</td>
<td>10%</td>
</tr>
<tr>
<td><strong>8. Energy per cycle per chip (#1x#5x#7)</strong></td>
<td>14 nJ</td>
<td>2.9 nJ</td>
</tr>
<tr>
<td><strong>9. Power (#4x#8)</strong></td>
<td>22 W</td>
<td>1.7 W</td>
</tr>
<tr>
<td><strong>10. Power Density (#9/#2)</strong></td>
<td>27 W/cm²</td>
<td>2.1 W/cm²</td>
</tr>
</tbody>
</table>

* These numbers are representative only and do not intend to reflect any existing device
Mobile Platform Goals & Challenges

• **Goal: Higher performance**
  – Challenge: How much power one can afford to spend in order to implement a performance feature?

• **Goal: Longer Battery life**
  – Challenge: How to balance the design for maximum performance and extended battery life?
Higher Performance vs. Longer Battery Life

- Processor average power is <10% of platform
- LCD and other components consume much more

➔ Even ideal processor can extend battery life by 11% at most!

➔ Decision:
  - Optimize for performance when Active
  - Optimize for battery life when idle

- Caveat
  - This observation is Pentium M specific. May not hold as such in the future!

Optimize for Performance

“Maximize performance at given thermal constraints”

Approximated by:
Maximizing performance at given Power budget

- The test:
  “A micro-architectural feature that gains performance or saves power should be better than simply using voltage/frequency scaling”

- That is:
  \[
  f \approx K \cdot V \\
  \text{Power} = \alpha \cdot C \cdot V^2 \cdot f \approx \alpha \cdot C \cdot f^3 \\
  \Delta \text{power/Power} = ((f + \Delta f)^3 - f^3)/f^3 \approx 3 \Delta f/f \\
  \text{Perf} = \text{IPC} \cdot f
  \]

- The right Performance/Power tradeoff:
  1% more performance in less than 3% Power – a gain!
Optimize for Battery Life

“Minimize Energy per Task”

• Should address both active and idle energy

• The active energy tradeoff:

\[
\text{Energy}_{\text{active}} = \text{Power}_{\text{active}} \times \text{Time}_{\text{active}}
\]

or

\[
\text{Energy}_{\text{active}} \approx \frac{\text{Power}_{\text{active}}}{\text{Perf}_{\text{active}}}
\]

→ The right Performance/Power tradeoff:

1% more performance in less than 1% Power – a gain!
Putting it all together: The Pentium M processor Approach

<table>
<thead>
<tr>
<th>Energy Loss</th>
<th>Energy Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constrained Perf Loss</td>
<td>Constrained Perf Gain</td>
</tr>
<tr>
<td>Wrong trade-off zone</td>
<td>Energy Breakeven line</td>
</tr>
</tbody>
</table>

 Performance loss  |  Performance gain 

Power Gain | Power Loss

All dates, plans, and features are preliminary and subject to change without notice
Back to Basics: “Less is More”

- Less instructions per task
- Less micro-ops per instruction
- Less transistor switches per micro-op
- Less energy per transistor switch.
“Less is More” in the Pentium M processor

- Less instructions per task
  - Advanced branch prediction, SSE instructions
- Less micro-ops per instruction
  - Micro-ops fusion
  - Dedicated stack engine
- Less transistor switches per micro-op
  - 1MB “power managed” L2 cache
  - the Pentium M processor bus
  - Various lower-level optimizations
  - Advanced clock gating
- Less energy per transistor switch
  - Enhanced Intel® SpeedStep® technology

Power-awareness top to bottom
Advanced Branch Prediction

• Typical today’s processors spend about $\frac{1}{4} - \frac{1}{3}$ of the time in branch misprediction recovery
  – Losing both performance and energy!

• The Pentium M processor employs best-in-class branch prediction
  – Uses Hybrid Bi-Modal/Global branch predictor
  – Loop detector
  – Indirect branch predictor

• Captures all standard program behaviors and new programming paradigms:
  – Loops of all iteration size
  – JITed and object oriented code

20% less mispredictions ➔ 7% performance gain*

* Relative to the Pentium M processor w/ traditional branch predictor (simulated)
**Dedicated Stack Manager**

- **IA32 instruction set provides explicit management of S/W stack**
  - E.g. PUSH, POP, RET, CALL

- **Stack management operations are an overhead**
  - E.g. Stack pointer increment
  - Normally done via machines main execution path

- **The Pentium M processor employs sophisticated H/W control for stack management**
  - Maintains/updates the stack pointer value in the decoder
  - Includes synchronization mechanism

- **Replaces a power hungry micro-op control**

**H/W management instead of power hungry Micro-ops**
Dedicated Stack Manager

Achieving >5% of Micro-op reduction
Micro-op Fusion – Best of all Worlds

• IA Instructions are typically broken into micro-ops
  – Normally handled individually

• Pentium M processor employs Micro-op fusion
  – Instructions with memory operands are fused
  – Single Micro-op during most of the instruction lifetime
  – Enhanced performance and power characteristics

• Micro-ops are split just in time for execution
  – Allows out-of-order, super-scalar execution
Micro-op Fusion – Best of all Worlds

add eax, dword ptr data

Decoder

Scheduler

Cache

ALU

Instruction execution flow diagram.
Micro-op Fusion – Best of all Worlds

Micro-op fusion enables effective machine utilization

Decoder

add eax, dword ptr data

LD + OP

Scheduler

LD + OP

Cache

LD

ALU

OP

Independent uOp OOO/Super-scalar execution

Achieving >10% of Micro-op reduction
Enhanced SpeedStep™ Technology

- The “Basic” SpeedStep™ Technology had
  - 2 operating points
  - Non-transparent switch

- The “Enhanced” version provides
  - Multi voltage/frequency operating points. The Pentium M processor 1.6GHz operation ranges:
    - From 600MHz @ 0.956V
    - To 1.6GHz @ 1.484V
  - Transparent switch
  - Frequent switches

- Benefits
  - Higher power efficiency
    - 2.7X lower frequency
    - 2X performance loss
    - >2X energy gain
  - Outstanding battery life
  - Excellent thermal mgmt.

![Graph showing Voltage, Frequency, Power relationship](image)
Performance Results

• 3 system
  – Intel® Pentium® M Processor (1.6 GHz/600 MHz)
  – Mobile Intel® Pentium® 4 Processor-M (2.4/1.2 GHz)
  – Mobile Intel® Pentium® III Processor-M (1.2 GHz/800 MHz)

• 3 operation modes
  – Always On (Max Frequency)
  – Portable/Laptop (Adaptive Frequency)
  – Maximum Battery (Min Frequency)

• 3 benchmarks
  – Mobile Representative Office Productivity Workload
  – Internet Experience workload
  – SPEC CPU 2000 V1.2

• Measured relative Performance and Efficiency
  – Efficiency = “energy per task” = Performance/average-power
Performance Results

Always On (Max Frequency)

- **Always on**
  - 2%-30% higher performance
  - 2X-3X efficiency

- **Portable**
  - Enhanced SpeedStep Technology ➔
  - 3X ➔ >4X efficiency in office

- **Maximum Battery**
  - Lower performance (15% or so)
  - 4X-5X efficiency on all benchmarks

Maximum Battery (Min Frequency)
Summary

The Intel Pentium M Processor

- A key component of the Intel Centrino™ Mobile Technology
- Exhibits Power awareness at all levels
- Provides breakthrough mobile performance and extended battery life
The End