

References CORDIC & Signal Processing

papers, WWW, books

June 1, 2004

1 papers – in CORDIC.doc/ (cp. Binder1.pdf)

- 00051651.pdf** A.A.J.de Lange, A J van der Hoeven, E.F.Deprettere, P.Dewilde, J.Bu: The Design of a 50MFLOP Arithmetic Chip for Massively Parallel Pipelined DSP Algorithms – The Floating Point Pipeline CORDIC Processor; 410–414
- 00084950.pdf** D.Timmermann, H.Hahn, B.J.Hosticka, G.Schmidt: A Programmable CORDIC Chip for Digital Signal Processing Applications; IEEE J. on Solid State Circuits, Vol 26, No 9, September 1991, 1317–1321
- 00100330.pdf** F.Piazza, M.Marchesi, G.Orlandi: A Fast DSP Circuit Based on FHT; ISCAS 1989 IEEE 216–219
- 00112264.pdf** E.F.Deprettere, A.A.J.de Lange, P.Dewilde: The Synthesis and Implementation of Signal Processing Applications Specific VLSI CORDIC Arrays; IEEE 1990 974–977
- 00112473.pdf** S.Naganathan, Yu Hen Hu: Architectural Design Styles in the VLSI Implementation of Real Discrete Fourier Transform; IEEE 1990 2316–2319
- 00116062.pdf** A.A.J.de Lange, E.F.Deprettere, A.van der Veen, J.Bu: Real Time Applications of the Floating Point Pipeline CORDIC Processor in Massively-Parallel Pipelines DSP Algorithms; IEEE 1990 1013–1016
- 00127956.pdf** Yu Hen Hu: The Quantization Effects of the CORDIC Algorithm; IEEE Trans. Signal Processing, Vol 40, No 4, April 1992 834–844
- 00127975.pdf** Yu Hen Hu, H.E.Liao: CALF – A CORDIC Adaptive Lattice Filter; IEEE Trans. on Signal Processing, Vol 40, No 4, April 1992, 990–993

- 00143467.pdf** Yu Hen Hu: CORDIC Based VLSI-Architectures for Digital Signal Processing; IEEE Signal Processing Magazine, July 1992 16–35
- 00143976.pdf** Jeong-A.Lee, Kiseon Kim: Discrete Fourier Transform Processor Using CORDIC; IEEE 1991 260–265
- 00150547.pdf** F.Kocsis: A Fully Pipelined, High Speed DFT Architecture; IEEE 1991 1569–1572
- 00176195.pdf** D.E.Metafas, G.E.Goutis: A Floating Point Pipeline CORDIC Processor with Extended Operation Set; IEEE 3066–3069
- 00190293.pdf** Gareth Dixon: An Array Processor Implementation of the CORDIC Algorithm; Plessey 5/1–5/8
- 00196976.pdf** Yu Hen Hu: The Quantization Effects of the CORDIC Algorithm; IEEE 1988 1822–1825
- 00204786.pdf** Jean Duprat, Jean-Michel Muller: The CORDIC Algorithm – New Results for Fast VLSI Implementation; IEEE Trans. on Computers, Vol 42, No 2, February 1993 168–178
- 00230290.pdf** Herbert Dawid, Heinrich Meyr: VLSI Implementation of the CORDIC Algorithm Using Redundant Arithmetic; IEEE 1992 1089–1092
- 00230356.pdf** Kiseon Kim, Jeong-A.Lee: VLSI Architectures for Image Processing and Address Mapping; IEEE 1992 1668–1671
- 00262301.pdf** Keith John Jones: Bit-Serial CORDIC DFT Computation with Multidimensional Systolic Processor Arrays; IEEE J. of Oceanic Engineering, Vol 18, No 4, October 1993 508–519
- 00266561.pdf** Hassan M.Ahmed: The Generalized Convergence Computation Method; IEEE 1989, 849–852
- 00266946.pdf** Vincent Cosidine: CORDIC Trigonometric Function Generator for DSP; IEEE 1989, 2381–2384
- 00266947.pdf** Hassan M.Ahmed, Kin-Ho Fu: A VLSI Array CORDIC Architecture; IEEE 1989, 2385–2388
- 00282100.pdf** Andy Peczalski, Paul Dietrich, Ross Mactaggart, David Grider: High-Throughput CORDIC Coprocessor for Signal and Display Processing; IEEE 1992, 564–567
- 00282701.pdf** Indradeep Gosh, Bandana Majumdar: Design of an Application Specific VLSI Chip for Image Rotation; Proc of the 7th Int. Conf. on VLSI Design, January 1994, IEEE 275–278

- 00315899.pdf** E.P.Mariatos, M.K.Birbas, A.N.Birbas: A Reconfigurable DSP Board Based on CORDIC Elements; IEEE 1994, 22–25
- 00365320.pdf** Yu Hen Hu, Zhenyang Wu: An Efficient CORDIC Array Structure for the Implementation of the Discrete Cosine Transform; IEEE Trans. on Signal Processing Vol 43, No 1, January 1995 331–336
- 00404460.pdf** Ramin Baghaie, Iiro Hartimo: An Efficient New Systolic Architecture for the Solution of the Discrete Cosine Transform; 453–461
- 00409249.pdf** E.P.Mariatos, D.E.Metafas, J.A.Hallas, C.E.Goutis: A Fast DCT Processor, Based on Special Purpose CORDIC Rotators; ??? 271–274
- 00479563.pdf** S.Freeman, M.O'Donnell: A Complex Digital Signal Processor Using CORDIC Rotators; IEEE 1995, 3191–3194
- 00502987.pdf** S.-J.Yih, M.Cheng, W.-S.Feng: Multilevel Barrel Shifter for CORDIC Design; Electronic Letters, 20th June 1996, Vol 32 No 13 1178–1179
- 00519575.pdf** F.El-Guibaly, A.Almulhem, A.Sabaa, D.Shpak: A High Speed CORDIC ALgorithm; IEEE 1995 485–488
- 00527527.pdf** R.Hamill, J.V.McCanny, R.L.Walke: Constant Scale Factor, On-line CORDIC Algorithm in the Circular Coordinate System; IEEE 1995 562–571
- 00541948.pdf** Sven Simon, Peter Rieder, Christian Schimpfle, Josef A.Nossek: CORDIC Based Architectures for the Efficient Implementation of Discrete Wavelet Transforms; IEEE 1996 77–80
- 00558371.pdf** S.Simon, P.Rieder, J.A.Nossek: Efficient VLSI Suited Architectures for Discrete Wavelet Transforms; IEEE 1996 388–397
- 00574510.pdf** A.Farina, L.Timmoneri: Parallel Algorithms and Processing Architectures for Space-Time Adaptive Processing; ???, 770–774
- 00588050.pdf** Shaoyun Wang, Vincenzo Piuri, Earl E.Schwartzlander,Jr.: A Unified View of CORDIC Processor Design; IEEE 1997, 852–855
- 00592206.pdf** Sathish Kumar, P and K M.M.Prabhu: Novel CORDIC-Based Systolic Arrays for the DFT and the DHT; IEEE 1997, 547–551
- 00599848.pdf** Seunghyeon Nahm, Wonyong Sung: A Fast Direction Sequence Generation Method for CORDIC Processors; IEEE 1997, 635–638
- 00604858.pdf** B.Haller, M.Streiff, U.Fleisch, R.Zimmermann: Hardware Implementation of a Systolic Antenna Array Signal Processor Based on CORDIC-Arithmetic; IEEE 1997, 4141–4144

- 00606820.pdf** Tomás Lang, Elisardo Antelo: CORDIC-based Computation of ArcCos and ArcSin; IEEE 1997, 132–143
- 00606822.pdf** Christian V.Schimpfle, Sven Simon, Josef A.Nossek: Low Power CORDIC Implementation Using Redundant Number Representation; IEEE 1997, 154–161
- 00659459.pdf** Hsiang-Ling Li, Chaitali Chakrabarti: Hardware Design of a 2-D Motion Estimation System Based on the Hough-Transform; IEEE Trans. on Circuits and Systems – II: Analog and Digital Signal Processing, Vol 45, No 1, January 1998, 80–95
- 00673651.pdf** Jie Chen, K.J.Ray Liu: A Complete Pipelined Parallel CORDIC Architecture for Motion Estimation; IEEE Trans. on Circuits and Systems – II: Analog and Digital Signal Processing, Vol 45, No 6, June 1998, 653–660
- 00750850.pdf** Oskar Mencer, Luc Semeria, Martin Morf, Jean-Marc Delosme: Application of Reconfigurable CORDIC Architectures; IEEE 1998, 182–186, also
<http://citeseer.ist.psu.edu/cache/papers/cs/4070/ftp:zSzzSzumunhum.stanford.eduzSzoskarzSzasil98.pdf/mencer00application.pdf>
- 00758297.pdf** Stephen McInerney, Richard B.Reilly: Hybrid/Multiplier/CORDIC Unit for Online Handwriting Recognition; International Conference On Acoustics, Speech, and Signal Processing, ICASSP '99, IEEE 1999, Vol 4, 1909–1912
- 00794460.pdf** Kees-Jan van der Kolk, Jeong-A Lee, Ed F.A.Deprettere: A Floating Point Vectoring Algorithm Based on Fast Rotations; ???
- 00822381.pdf** Martin Kuhlmann, Keshab K.Parhi: A High-Speed CORDIC Algorithm and Architecture for DSP Applications; IEEE 1999, 732–741
- 00831929.pdf** Martin Kuhlmann, Keshab K.Parhi: A Novel CORDIC Rotation Method for Generalized Coordinate Systems; IEEE 1999, 1361–1367
- 00867214.pdf** Tso Bing Juang, Shen Fu Hsiao: Low Power and Fast CORDIC Processor for Vector Rotation; IEEE Proc. 42nd Midwest Symposium on Circuits and Systems, MWSCAS '99, Aug. 1999, 81–83 Las Cruces
- 00871024.pdf** J.Villalba, J.Hormigo, M.A.González, E.L.Zapata: MMX-like Architecture Extension to Support the Rotation Operation; IEEE International Conference on Multimedia and Expo, ICME 2000, New York, July 30 - August 2, IEEE 2000, Vol III, 1383–1386
- 00886732.pdf** Javier Valls, Martin Kuhlmann, Keshab K.Parhi: Efficient Mapping of CORDIC Algorithms on FPGA; IEEE 2000, 336–345

- 00887154.pdf** Jae-Hyuck Kwak, Vincenzo Piuri, Earl E.Schwartzlander,Jr.: Fault-Tolerant High-Performance CORDIC Processor; International Symposium on Defect and Fault Tolerance in VLSI Systems, DFT 2000, October 25 - 27, 2000 Yamanashi, Japan IEEE 2000, 164–172
- 00911589.pdf** Joe Costello, Damin-Al Khalili: Behavioural Synthesis of Low Power Floating Point CORDIC Processors; International conference on Electronics, Circuit and Systems, ICECS '00, December 2000, Lebanon, IEEE 2000, 506–509
- 00941147.pdf** An-Yeu Wu, Cheng-Shing Wu: A Unified Framework for Vector Rotational CORDIC Family Based on Angle Quantization Process; IEEE 2001, 1233–1236
- 00944473.pdf** Jie Chen, K.J.Ray Liu: Efficient Architecture and Design of an Embedded Video Coding Engine; IEEE Trans. on Multimedia, Vol 3, No 3, September 2001, 285–297
- 00949836.pdf** Yi Yang, Chunyang Wang, M.Omair Ahmad, M.N.S.Swamy: An Online CORDIC-Based 2-D IDCT Implementation Using Distributed Arithmetic; Proc. Int. Symposium on Signal Processing and its Applications, IEEE 2001, 296–299
- 00972492.pdf** Sungwook Yu, Earl E.Schwartzlander,Jr.: A Scaled DCT Architecture With the CORDIC Algorithm; IEEE Trans. on Signal Processing, Vol 50, No 1, January 2002, 160–167
- 00982606.pdf** Wu Zhilu, Ren Guanghui, Zhao Yaqin: A Study on Implementing Wavelet Transform and FFT with FPGA; IEEE 2001, 486–489
- 00987043.pdf** Tomás Lang, Elisardo Antelo: High-Throughput 3D Rotations and Normalizations; IEEE 2001, 846–851
- 01032874.pdf** B.Das, S.Banerjee: Unified CORDIC-Based Chip to Realise DFT/DHT/DCT/DST; IEE Proc. Comput. Digit. Tech., Vol 149, No 4, July 2002, 121–127
- 01049716.pdf** Jeongseon Euh, Jeevan Chittamuru, Wayne Burleson: CORDIC Vector Interpolator for Power Aware 3D Computer Graphics; IEEE Workshop on Signal Processing Systems, SIPS2002, IEEE 2002, 240–245
- 01169138.pdf** Tze-Yun Sung, Yu-Hen Hu, H.J.Yu: Doubly Pipelined CORDIC Array for Digital Signal Processing Algorithms; ICASSP, 1986, Tokyo, IEEE 1986, 1169–1172
- 01171404.pdf** Daniel T.L.Lee, Martin Morf: Generalized CORDIC for Digital Signal Processing; IEEE 1982, 1748–1751

- 01197049.pdf** David Defour, Florent de Dinechin, Jean-Michel Muller: A New Scheme for Table-Based Evaluation of Functions; IEEE 2002, 1608–1612
- 01202356.pdf** Bipul Das, Swapna Banerjee: A Low Complexity Architecture for Complex Discrete Wavelet Transform; ICASSP 2003, IEEE 2003, II-309–II-312
- 01202362.pdf** Miloš Krstić, Alfonso Troya, Koushik Maharatna, Eckhard Grass: Optimized Low Power Synchronizer Design for the IEEE 802.11a Standard; International Conference on Acoustics, Speech, and Signal Processing, ICASSP 2003, April 2003, Hong Kong, IEEE 2003, II-333–II-336
- 01206137.pdf** Chuen-Yau Chen, Wen-Chih Liu: Architecture for CORDIC Algorithm Realization Without ROM Lookup Tables; IV-544–IV-547
- 01224848.pdf** A.Khayatzadeh, H.S.Shahhoseini, M.Naderi: Systolic CORDIC DCT: An Effective Method for Computing 2D-DCT; IEEE 2003, 193–196
- 01244147.pdf** T.Sansaloni, A.Pérez-Pascual, J.Valls: Area-Efficient FPGA-Based FFT Processor; Electronic Letters 18th September 2003, Vol 39 No 19
- 01261966.pdf** Shen-Fu Hsiao, Yu-Hen Hu, Tso-Bing Juang: A Memory-Efficient and High-Speed Sine/Cosine Generator Based on Parallel CORDIC Rotations; IEEE Signal Processing Letters, Vol 11, No 2, February 2004, 152–155
- 30.pdf** Javier Oscar Giacomantone: Tradeoffs in Arithmetic Architectures for CORDIC Algorithm Design; ???
- 00.pdf**

2 WWW

- Sven Simon, Peter Rieder, Christian V. Schimpfle, Josef A. Nossek: CORDIC Based Architectures for the Efficient Implementation of Discrete Wavelet Transforms; IEEE International Symposium on Circuits and Systems, IS-CAS 1996 Vol 4 77–80
- Christian V. Schimpfle , Sven Simon , Josef A. Nossek: Low Power CORDIC Implementation Using Redundant Number Representation; Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP '97), July 14–16, IEEE 1997 154–161

Peter Rieder, Sven Simon, Christian V. Schimpfle: Application Specific Efficient VLSI Architectures for Orthogonal Single- and Multiwavelet Transform; J. VLSI Signal Processing – Systems for Signal, Image, and Video Technology, Vol 21, No 2, 77–90 (1999)

simon_m_g_w_b.pdf S.Simon, M.Müller, H.Gryska, A.Wortmann, S.Buch: An Instruction Set for the Efficient Implementation of the CORDIC Algorithm; IEEE International Symposium on Circuits and Systems, ISCAS 2004

Neil Eklund: CORDIC – Elementary Function Computer Using Recursive Sequences;
<http://archives.math.utk.edu/ICTCM/EP-11/C27/paper.pdf>

Ray Andraka: A Survey of CORDIC Algorithms for FPGA based Computers;
www.fpga-guru.com/files/crdcsrvy.pdf

Helmut Knaust: How Do Calculators Calculate?
www.math.utep.edu/Faculty/Helmut/wcordic.html

??? Square-root based on CORDIC; ARCTAN(x) using CORDIC;
www.restena.lu/concict/Jeunes/Math/square_ROOT_cordic.htm

Grant G.Griffin: CORDIC FAQ; www.dspguru.com,
www.dspguru.com/info/faqs/cordic.htm,
www.dspguru.com/sw/opensp/alglib.htm

Pitts Jarvis: Implementing CORDIC Algorithms; Dr. Dobbs Journal
www.ddj.com/print/documentID=14896

3 books

S.Y.Kung: VLSI Array Processors; Prentice Hall, 1988